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Enclosed herewith for filing is a patent application, as follows:

Inventor(s): Chen et al.

Title: Read and Erase Verify Methods and Circuits Suitable for Low Voltage Non-Volatile Memories

X	Return Receipt Postcard
X	This Transmittal Letter (in duplicate)
13	page(s) Specification(not including claims)
3	page(s) Claims
1	page Abstract
5	Sheet(s) of Drawings
2	page(s) Declaration For Patent Application and Power of Attorney
	page NonPublication Request
2	page(s) Recordation Form Cover Sheet (in duplicate)
1	page(s) Assignment

CLAIMS AS FILED

	Number Filed			Number Extra		Rate			Basic Fee
For Total Claims	19	-20	=	0	x	$18.00	=	$	750.00
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Independent Claims	3	-3	=	0	x	$84.00	=	$	0.00
☐ Fee of ____ for the first filing of one or more multiple dependent claims per application								$	
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Respectfully submitted,

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READ AND ERASE VERIFY METHODS AND CIRCUITS SUITABLE FOR LOW VOLTAGE NON-VOLATILE MEMORIES

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Khandker Quader

FIELD OF THE INVENTION

[0001] This invention relates generally to non-volatile memories and their operation, and, more specifically, to techniques.

BACKGROUND OF THE INVENTION

[0002] The principles of the present invention have application to various types of non-volatile memories, those currently existing and those contemplated to use new technology being developed. Implementations of the present invention, however, are described with respect to a flash electrically-erasable and programmable read-only memory (EEPROM), wherein the storage elements are floating gates.

[0003] A number of architectures are used for non-volatile memories. A NOR array of one design has its memory cells connected between adjacent bit (column) lines and control gates connected to word (row) lines. The individual cells contain either one floating gate transistor, with or without a select transistor formed in series with it, or two floating gate transistors separated by a single select transistor. Examples of such arrays and their use in storage systems are given in the following U.S. patents and pending applications of SanDisk Corporation that are incorporated herein in their entirety by this reference: Patent Nos. 5,095,344, 5,172,338, 5,602,987, 5,663,901, 5,430,859, 5,657,332, 5,712,180, 5,890,192, and 6,151,248, and Serial Nos. 09/505,555, filed February 17, 2000, and 09/667,344, filed September 22, 2000.

[0004] A NAND array of one design has a number of memory cells, such as 8, 16 or even 32, connected in series string between a bit line and a reference potential through select transistors at either end. Word lines are connected with control gates of cells in different series strings. Relevant examples of such arrays and their operation are given in U.S. patent 6,046,935

and U.S. patent application Serial No. 09/893,277, filed June 27, 2001, that are also hereby incorporated by reference, and references contained therein.

[0005] In non-volatile semiconductor memories, such as an EEPROM or Flash memory, the amount of data stored per memory cell has been increased in order to increase storage densities. At the same time, the operating voltages of such devices have decreased to reduce power consumption. This results in a greater number states stored in a smaller range of voltage or current values. As the voltage or current separation between data states decreases, the accurate placement of the breakpoints used to distinguish between data states becomes more critical. Another complicating factor is that the parameter, such as threshold voltage, representing the data state of the storage element populations can vary with operating conditions. Consequently, in order to maintain the reliability of memory operation in light of the confilicting demands of incresing the number of states per cell and decreasing operating voltages, improvents to memory design become ever more important.

[0006] Figure 1 shows a distribution of threshold voltages for a collection of storage elements programmed into one of four data states for a system designed for 3 volt operations, such as described in U.S. patent 6,046,935 and U.S. patent application Serial No. 09/893,277, both incorporated above. The programming process has grouped the memory cells into four populations, labeled as "0", "1", "2", and "3". The "0" state is characterized by a negative threshold voltage, V_{th}<0V, with the other states characterized by having threshold voltages above ground. Typically, the following an erase and pre-programming phase, the memory elements are programmed to their respective data states based upon the verify voltages of VCG1V for the "1" state, VCG2V for the "2" state, and VCG3V for the "3" state. The result is the four cell population distributions represented by the lumps in Figure 1.

[0007] During a read process, the data states are distinguished from each other by the breakpoints: VCR3R distinguishes the "3" state from the "2" ,VCR2R distinguishes the "2" state from the "1" , and VCR1R distinguishes the "1" state from the "0". Although the states are defined by their threshold voltages in the exemplary embodiment of a FLASH memory, another parameter, such as current or frequency, may be sensed in a read or verify operation. More detail on read, write, and verify operations are given in the various references incorporated above and

in U.S. patent application Serial No. 10/052/924, filed on January 18, 2002, that is also hereby incorporated by reference, and references contained therein.

[0008] To maintain the integrity of both the read and the write process, both the population distributions of cells in the different states and the read points for distinguishing these points need to be well defined. The population distributions can shift over time or as operating conditions (temperature, power supply level, device age, etc.) change. Although the four-state, 3.0V design (corresponding to Vdd=2.6V) may provide a sufficient safety margin in which to place the read points between the state populations, these tolerances can become very tight as systems move to more states, lower operating voltages, or both.

SUMMARY OF THE INVENTION

[0009] According to a primary aspect of the present invention, a non-volatile memory wherein the sensing process compensates for the variations of all of the populations of the memory cells due to operating conditions. The read parameter used to distinguish the data states characterized by a negative threshold voltage from the data states characterized by a positive threshold voltage is compensated for the memory's operating conditions, rather than being hardwired to ground. This allows for a more efficient budgeting of the available voltage widow, which is particularly important in multi-state memories designed for low voltages operation. The compensation for operating conditions can also be applied to the program verify parameter for the lowest, non-negative threshold state. In an exemplary embodiment, the read parameter for the data state with the lowest threshold value above ground is temperature compensated to reflect the shifts of the storage element populations on either side of the read parameter.

[0010] According to another aspect of the present invention, an erase process is presented that can take advantage the operating condition compensated sensing parameter. As the sensing parameter is no longer fixed at a value corresponding to 0 volts, instead shifting according to operating conditions, a sufficient margin is provided for the various erase verify levels even at lowered operating voltages.

[0011] In an exemplary embodiment, a 1.8 volt design uses a temperature compensated read parameter to distinguish between a negative threshold data state and the lowest of the positive

threshold states. This is achieved by producing a temperature compensated control gate voltage in a range of 0-0.2 voltage provided, in one embodiment, by a negative voltage source connected to a band gap generator. This provides move overhead in which to use a number of verify levels associated with as erase and soft-programming process.

[0012] Additional aspects, features and advantages of the present invention are included in the following description of exemplary embodiments, which description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figure 1 shows a distribution of threshold voltages for a collection of storage elements programmed into one of four data states for a system designed for 3-volt operations.

[0014] Figure 2 illustrates the effect of operating conditions on a memory system.

[0015] Figures 3 shows the use an operating condition compensated read voltage for distinguishing between states characterized by negative and positive voltages.

[0016] Figure 4 is a flowchart for an exemplary embodiment of a preprogramming erase process.

[0017] Figure 5 shows an arrangement of various erase verify levels in an exemplary embodiment.

[0018] Figure 6 is a block diagram of a memory system incorporating aspects of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0019] For specificity, the present invention will be described mainly in terms of a 4-state, 1.8V (Vdd=1.5V) design with a first state characterized by a negative V_{th} value and one or more (here 3) states characterized by a V_{th}>0V. More generally, there will be one or more states characterized by a negative threshold and be one or more states characterized by a positive threshold. When reference to a specific memory system is needed, the exemplary embodiment is a flash memory composed of units having one or more floating gates and usually one or more

select gates; for example, a memory of the NAND type that is composed of strings of floating gate transistors connected in series with a select gate on either end. Various applicable memory structures are described in the reference incorporated into the Background section.

[0020] Figure 2 illustrates the effect of operating conditions on a memory system. This figure again shows three state populations ("1", "2", "3") characterized by a positive threshold value and one population ("0") characterized by a negative threshold value. The solid lines ("0", "1", "2", "3") represent the distribution of the cells as initial programmed for the four states based on verify levels determined by reference cells, a band-gap device, or other techniques. The dotted lines ("0′ ", "1′ ", "2′ ", "3′ ") represent the distributions shifted due to a change in operating conditions. Examples of such changes in operating conditions are power supply variations, device aging, temperature variations, and so on. For specificity, the temperature variation case is mainly discussed here; for example, in a particular variety of flash memory cells, it is found that the populations shift by something on the order of 0.25V over the temperature range of –40°C to +100°C, or about 1.8mV/°C. If the temperature range is a less extreme –10°C to +85°C, this is still a shift of 0.17V. The spread of the three positive threshold populations, sufficient room between the populations to be able to distinguish the distributions, and additional room to allow for the population shifts due to operating conditions all need to fit between 0V and Vdd=1.5. Allowing up to a quarter volt of population shift for each population significantly cuts into the voltage window. (A possible alternative involves the use of charge pumps to increase the size of the voltage window relative to the power supply level, but this is often too expensive to be practical.)

[0021] The space available is also squeezed from below 0V as the operating voltages are decreased. To use of a lower Vdd value to use less energy usually leads to a less negative voltage for the distribution of storage elements subsequent to an erase process. This leaves less room for any soft programming or other verify levels discussed below to fit in below the 0V level that distinguishes the "0" state from the "1" state.

[0022] The read point used to distinguish between the "2" and "3" state is shown as VR3 and the read point used to distinguish between the "1" and "2" state is shown as VR2. When the population distributions shift, they become too close to the read points to maintain a sufficient

margin to safely read the data within the restricted space in the of the threshold windows. Consequently, techniques have been introduced to vary the read points to VR2′ and VR3′ according to operating conditions. (Although this is discussed in terms of voltages, the actual quantity used in the sensing process may be current or another parameter, as noted in the Background.) For example, for the sort of temperature variation described above, if the V_{read} and V_{verify} levels vary as $V_{read}/V_{verify} \sim V_{T=0}+(1.8mV/°C)\ T(°C)$, where $V_{T=0}$ is the read/verify value at 0°C, the sense point will be shifted along with the population distributions. This frees up much of the amount of the population shift to be used for population spread and read margin. The use of reference or tracking cells, such as described in U.S. patent number 5,172,338 or U.S. patent application serial number 09/671793 filed September 27, 2000, which are both hereby incorporated by reference, is one method for handling this problem. Other techniques for compensation due to operating conditions are described in U.S. patent application serial number 10/053,171 filed November 2, 2002, and U.S. Patent number 5,694,356, both hereby incorporated by reference.

[0023] The prior art distinguishes the "0" state, characterized by a negative threshold voltage, from the "1" state, characterized by a positive threshold voltage, by use a read point VR1 hardwired to ground. The use of VR1=0V is particularly easy to implement and clearly distinguishes between the highest of any negative threshold voltage states and the lowest of any positive threshold states; for example, the system can just set the control gate to ground and see if any current flows. Consequently, in the prior art VR1′ is the same as VR1 since VR1 is not a function of temperature, $VR1'=VR1\neq f(T)$. Additionally, temperature compensation is harder around V=0, whether for VR1 or another parameter. However, this results requiring a relatively large gap 201 between the lower end of the "1" state population (as determined by the verify level for this state when first programmed) and V=0, further squeezing the available space.

[0024] A major aspect of the present invention is to introduce compensation for operating conditions for the breakpoint that distinguishes the negative threshold states from the positive threshold states, rather than just a hardwired value of 0V. Thus, in the temperature example, the fixed, hardwired VR1=0V read point is replaced by a temperature compensated value, VR1=f(T), more fully using the available voltage window. This can be used to add more states, make the memory more robust, relax margins elsewhere, or some combination of these as

selected by the designer. As described further below, this also allows more space for the various negative voltage values.

[0025] Figure 3 illustrates the use of a condition compensated breakpoint for distinguishing a V_{th}<0V state from a V_{th}>0V state, where, for simplicity, only a single negative threshold state ("0") and a single positive threshold state ("1") are shown. As before, the dotted lines ("0′", "1′", "2′", "3′") represent the distributions shifted due to a change in operating conditions from the solid distributions ("0", "1"). In contrast to the prior art, whereas the read level VR1 would correspond to the 0V axis, the present invention introduces a read value VR1 corresponding to the operating conditions of the solid distributions that is offset to a positive voltage value that shifts along with the distributions, such as VR1′ corresponding to the conditions of the distributions with the dotted lines. For example, the temperature dependence of VR1 can be designed to track that of the storage elements.

[0026] Compensation for operating conditions can also be applied to the verify level for the "1" state, V_{ver1}. This may be the same level as used for the read operation or offset by a margin above the read value, as is described in many of the references incorporated above; see, for example, U.S. patent number 5,418,752. Thus, V_{ver1} may also be function of operation conditions, where a $V_{ver}1$ would correspond to the operating conditions for the "0" and "1" population distributions and a $V_{ver}1'$ would correspond to the conditions for the "0′" and "1′" distributions.

[0027] The use of a sensing parameter compensated for operating conditions for use between the positive threshold states and the negative threshold states frees up more room in the available voltage window. Whereas in the fixed, VR1=0V embodiment shown in Figure 2 the gap 201 between the "1" states and 0V always had to be large enough so that the "1" states were above 0V with sufficient margin and, independently, the gap 203 between the "0" states and 0V always had to be large enough so that the "0" states were below 0V with sufficient margin, according to the invention as illustrated in Figure 3, it is only necessary the total gap 301 between the "0" and "1" distribution is large enough to be able to distinguish elements of the two populations with sufficient fidelity. This extra usable space in the voltage window can also be used to provide sufficient space to fit in the various erase verify levels associated establishing the V_{th}<0V

populations that are described below with respect to Figure 4.

[0028] Although the discussion here is being presented in terms of voltages, such as VR1, being used as the sensing parameter (whether during a read or during a verify) since voltage is what distinguishes the "0" states from the "1" states, other parameters such as current or frequency may also be used, as described more fully is U.S. patent application serial number 10/052,888 filed January 18, 2002, which is hereby incorporated by reference.

[0029] Figure 4 is a flow chart of an exemplary embodiment of an erase and program operation that illustrates some of levels that may be used in preparing the "0" or ground state in the storage elements, both for when this is the target value of a storage element and also as a possible starting point for programming a storage unit into the data states characterized by a positive threshold voltage. This process starts at step 401.

[0030] Step 401 pre-programs the storage units. This serves the dual purpose of having the storage units start the actual erase 405 at a more uniform state and also helps to even wear so that the cells age more uniformly. For example, in a NAND architecture, such as that described in U.S. patent 6,046,935 and U.S. patent application Serial No. 09/893,277 incorporated above, this can be implemented by taking all of the wordlines in the erase unit high for a single pulse of, say, 10μs. Other architectures or cell types would use the appropriate programming technique when this step is included.

[0031] The actual erase takes place in step 405. This will again be as appropriate for the storage element and architecture. For the exemplary NAND flash EEPROM, this can be the application of the erase voltage to the memory's well structure, such as an application of 18V for around 1ms. The success of the erase operation can be checked in an erase verify operation, step 407. This checks whether all of the erased storage elements have a threshold voltage below a value V_{EV1}<0V. If any storage elements fail to verify, they can either be logically remapped or subjected to further erasing, as show by the NO loop.

[0032] In one exemplary embodiment, the result post-erasure population will not necessarily correspond to the "0" or ground state. This is shown in Figure 5 as the population 501. The result of the erase process generally results in a population with more spread than is desired, both

because it results in a less well defined state and also because it represents a less uniform starting point from which to program the memory cells to higher states. Consequently, this exemplary embodiment also includes a soft-programming made up of steps 411, 413, or 415.

[0033] In a soft-programming process, the storage elements are gradually raised from their initial, post-erasure distribution 501 to the ground or "0" state 503. In the exemplary flash memory embodiment, this typically consists of a programming pulse (step 411), often using lesser voltages than in regular programming, whose result is then verified with a reference parameter (here a voltage V_{EV2} in step 413). This continues until a certain number of cells, which can be a settable parameter, exceed the verify level V_{EV2} (step 415). In a variation, the soft-programming process can also include the lockout from further programming of cells that verify correctly, as is discussed in U.S. patent application 10/068,245, filed 02/06/2002, entitled "Implementation of an inhibit during soft programming to tighten an erase VT distribution" by Feng Pan and Tat-Kwan Edgar Yu, which is hereby incorporated by reference.

[0034] Since in some embodiments the soft-programming may continue until a number of storage elements' threshold exceed V_{EV2}, the fastest programming elements in the "0" population 503 will extend the top end population beyond this level. To insure that it does not extend too high, an additional verify level V_{autoEV} can be used to check this in step 417. At this point the status of the device can be reported out and the writing of data in step 419 taking the states not to remain in the "0" state to their target values.

[0035] The process of Figure 4 is again just an exemplary embodiment and, even for a flash memory embodiment, there are many variations. For example, some of the verifies may be omitted. In particular, it is usually found that a memory behaves well enough so that the extra verify of step 417 is not required.

[0036] Returning to Figure 5, 501 is the post-erasure distribution and 503 is the same set of storage elements after soft-programming. At this point, distribution 503 contains not just those cells whose target state is "0", but also those cells that will subsequently be programmed into the higher data states, such as the "1" distribution shown at 505. It is the various verify voltages (V_{EV1}, V_{EV2}, V_{autoEV}) of Figures 4 and 5 need to fit below 0V in the prior art. As with VR1 and the other reference voltages above 0V, less space is available for the negative reference values of

these erase verify voltages as the voltage window shrinks.

[0037] A number of techniques are known for reading non-negative threshold voltage levels. For example, a bit line can be pre-charged and a voltage level applied to a cell's control gate and determining whether the bit line discharges, a process described in more detail in U.S. patent number 6,317,363 that is hereby incorporated by reference. In the example of a NAND type memory, the bit line would be pre-charged from the source side of the NAND chain, the non-selected storage elements would have applied an over-drive voltage applied so that they are fully turned on, and the selected cell would have a control gate voltage appropriate to the threshold level to be measured. Such a technique will not work for a determining a cell's threshold voltage having a negative value, such as those related to the various erase verify levels described herein. One technique for determining negative threshold values, again described in the context of a NAND architecture, is to apply a voltage (such as V_{dd}) to the source side of the NAND chain, with the non-selected storage elements again turned fully on. A voltage level can then be applied to the selected cell's control gate such that if the threshold voltage is low enough, the cell will conduct due to the body bias.

[0038] Tables 1 and 2 present exemplary values for a control gate voltage (V_{CG}) and the threshold value of the highest cell in the result population that would verify at this value. They also present a read value for the lowest positive threshold value, VR1. The values of Table 1 corresponds to 3 volt design, such as is described in the Background section, while those of Table 2 correspond to the 1.8 volt design of the exemplary embodiment. In both of these tables, it should be noted that the "Highest Cell V_{th}" values of the storage cells are estimates.

	V_{CG}	Highest Cell V_{th}
V_{EV1}	0V	–0.8V
V_{EV2}	0.45V	–0.5V
V_{autoEV}	0.65V	–0.3V
VR1	0V	0V

Table 1

[0039] As shown in Table 1, the prior art reads the "1" state with a control gate voltage 0 volts by connecting it to ground, resulting in the VR1 shown in Figure 2. A design with Vdd=2.6V allows for an erase voltage to take the storage elements below a value of V_{EV1}<–0.8V for the post-erasure population 501. This allows a 0.8 volt window between V_{EV1} and VR1 into which the V_{EV2} and V_{autoEV} be fit, here respectively at –0.5V and –0.3V. These threshold values correspond to placing Vdd on the drain of the cell and V_{CG} on the control gate and using the body bias of the cell.

[0040] For a 1.8 volt design, the post-erasure population 501 is not moved as far into the negative voltage region. In particular, the exemplary embodiment again uses V_{CG}=0V for the initial erase verify, but now the highest cells in the distribution will be only about half a volt below ground, V_{EV1} = –0.5V. Consequently, this allows a widow of only half a volt into which to soft program the post erasure population and form the "0" state (503, Figure 5) if the hardwiring of VR1 to ground is maintained. This is shown in Table 2 that gives also gives an exemplary value for V_{EV2} and the optional V_{autoEV}, where the same V_{CG} are used as in Table 1, but the verify levels now fit into the smaller available voltage widow.

	V_{CG}	Highest Cell V_{th}
V_{EV1}	0V	–0.5V
V_{EV2}	0.45V	–0.25
V_{autoEV}	0.65V	–0.05V
VR1(T)	0V-0.2V	0V-0.2V

Table 2

[0041] Table 2 also shows a range of values of VR1 due to temperature compensation in the exemplary embodiment. As described previously, by compensating the read parameter, verify parameter, or both for the "1" state, the present invention only requires that the total space between the "0" and the "1" distribution (301 of Figure 3) as these shift according to operating conditions is sufficiently large to insure data fidelity. In contrast, the prior art required that both the space between both the bottom of the "1" and the top of the "0" distribution and the fixed VR1=0V value (201 and 203, respectively, Figure 2) is sufficiently large to insure data fidelity,

independently of each other and independently of shifts in the distributions due to operation conditions. As the values of Table 2 show, the allowable space within the voltage window allows very little to be budgeted to insuring the "0" population could stay below a fixed VR1=0V value.

[0042] Referring to Figure 6, a block diagram of an example memory system 10 incorporating aspects of the present invention is shown. Memory system 10 includes a large number of individually addressable memory cells arranged in a regular array 11 of rows and columns, although other physical arrangements of cells are possible. Bit lines (not shown in Figure 6) extend along columns of array 11 and are connected to a bit line decoder and driver circuit 13 through lines 15. In exemplary embodiment, the memory cell array can be of the NAND or NOR type described in the references incorporated by reference above. Word lines (again not shown in Figure 6) extend along rows of array 11 and are connected through lines 17 to a word line decoder and driver circuit 19. Steering gate lines (also not shown in Figure 6) may extend along columns of array 11 and are connected to a steering gate decoder and driver circuit 21 through lines 23.

[0043] Each of the decoders 13, 19 and 21 receives memory cell addresses over a bus 25 from a memory controller 27. The decoder and driver circuits are also connected to controller 27 over respective control and status signal lines 29, 31 and 33. Voltages applied to the steering gates and bit lines are coordinated through a bus 22 that interconnects the decoder and driver circuits 13 and 21.

[0044] Controller 27 is connectable through lines 35 to a host device (not shown). The host may be, for example, a personal computer, notebook computer, digital camera, audio player, or any of various other hand-held electronic devices. The memory system of Figure 6 will commonly be implemented in a card according to one of several existing physical and electrical standards, such as the standards set by the PCMCIA, the CompactFlash™ Association, the MMC™ Association or the Secure Digital (SD) Card Association. When in a card format, the lines 35 terminate in a connector on the card which interfaces with a complementary connector of the host device. The electrical interface of many cards follows the ATA standard, wherein the memory system appears to the host as if it were a magnetic disk drive. Other memory card

interface standards also exist. Alternatively to the card format, memory systems of the type shown in Figure 6 are embedded in the host device.

[0045] Figure 6 also shows reference voltage generator 47. As noted above, compensation for operating conditions around 0 volts can not be readily implemented by traditional methods, such as a band gap generator. Another technique used for compensation is a resistor divider; however, aside from the disadvantage of being a current sink, such a divider may not be stable at low voltage levels and is again not suitable for use near V_{CG}=~0V.

[0046] In one exemplary embodiment, the reference voltage generator 47 can include a band gap generator connected to a negative voltage source, which would produce a negative voltage level from the power supply, thereby allowing the band gap generator to supply the needed VR1 values near 0 volts. (Details on band gap generators are described, for example, in "Analog Integrated Circuit Design", David A. Johns and Ken Martin, John Wiley & Sons, 1997, which is hereby incorporated by this reference.) Although Figure 6 schematically shows the reference voltage generator 47 on the same memory device as the memory array, either one or both of the band gap generator or the negative voltage generator can be on another chip in the memory system from which the voltage levels would then be supplied.

[0047] Although the various aspects of the present invention have been described with respect to specific embodiments, it will be understood that the invention is protected within the full scope of the appended claims.

IT IS CLAIMED:

1. A memory comprising:

a non-volatile data storage element capable of storing a first data state characterized by a negative threshold voltage and one or more second data states characterized by a positive threshold voltage; and

sense circuitry connectable to the data storage element that can distinguish the data state of the storage element, comprising;

a compensation circuit, whereby the parameter used by the sense circuit to distinguish between the first and second data states is compensated based on operating conditions.

2. The memory of claim 1, wherein said operating conditions comprise temperature.

3. The memory of claim 1, wherein said operating conditions comprise the voltage level of an external power supply.

4. The memory of claim 1, wherein said data storage element is capable of storing a plurality of said second data states.

5. The memory of claim 1, wherein said parameter is a voltage.

6. The memory of claim 1, wherein said parameter is in a range of from 0 volts to 0.2 volts.

7. The memory of claim 1, wherein said parameter is a current.

8. The memory of claim 1, further comprising:

write circuitry connectable to the data storage element and the sense circuitry, wherein the sense circuitry is used for program verify and the verify level for the second data states is compensated based on operating conditions.

9. The memory of claim 1, further comprising:

a negative voltage source; and

a band gap generator connectable to the negative voltage source whereby said parameter is provided.

10. The memory of claim 9, wherein said parameter is a voltage and said band gap generator provides a voltage in the range of 0 volts to 0.2 volts.

11. A method of operating a non-volatile memory, comprising:

selecting a data storage element storing one of a plurality of data states, said plurality of data states comprising a first data state characterized by a negative threshold voltage and one or more second data states characterized by a positive threshold voltage;

providing a sensing parameter, wherein said sensing parameter is compensated for operating conditions; and

using said sensing parameter to distinguish between the first data states and the second data states.

12. The method of claim 11, wherein said plurality of data states comprises a plurality of second data states.

13. The method of claim 11, wherein said operating conditions comprise temperature.

14. The method of claim 11, wherein said operating conditions comprise the voltage level of an external power supply.

15. The method of claim 11, wherein said sensing parameter is a voltage.

16. The method of claim 15, wherein said sensing parameter is a voltage in the range of 0 volts to 0.2 volts.

17. The method of claim 11, wherein said sensing parameter is a current.

18. The method of claim 11, further comprising:

generating a negative voltage, wherein the sensing parameter is produced using said negative voltage.

19. A non-volatile memory device, comprising:

means for storing a data value selected from a plurality of data states, a first of which is characterized by a negative threshold value and a second of which is characterized by a positive threshold value;

means for compensating a parameter for the operating conditions of the memory device; and

means for distinguishing between said first data state and said second data state by use of said compensated parameter.

READ AND ERASE VERIFY METHODS AND CIRCUITS SUITABLE FOR LOW VOLTAGE NON-VOLATILE MEMORIES

ABSTRACT OF THE DISCLOSURE

[0048] In a non-volatile memory, the read parameter used to distinguish the data states characterized by a negative threshold voltage from the data states characterized by a positive threshold voltage is compensated for the memory's operating conditions, rather than being hardwired to ground. In an exemplary embodiment, the read parameter for the data state with the lowest threshold value above ground is temperature compensated to reflect the shifts of the storage element populations on either side of the read parameter. According to another aspect, an erase process is presented that can take advantage the operating condition compensated sensing parameter. As the sensing parameter is no longer fixed at a value corresponding to 0 volts, instead shifting according to operating conditions, a sufficient margin is provided for the various erase verify levels even at lowered operating voltages.

Attorney Docket No.: M-12649 US

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

READ AND ERASE VERIFY METHODS AND CIRCUITS SUITABLE FOR LOW VOLTAGE NON-VOLATILE MEMORIES

which (check) ☒ is attached hereto.

☐ and is amended by the Preliminary Amendment attached hereto.

☐ was filed on as Application Serial No.

☐ and was amended on (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			☐	☐

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Attorney Docket No.: M-12649 US

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

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Inventor's Signature: Jian Chen Date: 4/8/03
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Sunnyvale, CA 94087
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Full name of sole (or joint) inventor:
Inventor's Signature: _____ Date: _____
Residence:
Post Office Address: Citizenship:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Jian Chen and Khandker Quader		
Assignee:	SanDisk Corporation		
Title:	Read and Erase Verify Methods and Circuits Suitable for Low Voltage Non-Volatile Memories		
Application No.:	Unknown	Filing Date:	Herewith
Examiner:	Unknown	Group Art Unit:	Unknown
Docket No.:	M-12649 US	Conf. No.:	Unknown

Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST

Sir:

The above-identified assignee, a Delaware corporation, hereby revokes all powers of attorney previously given and appoints the attorney(s) and/or agent(s) identified by the following Customer Number to prosecute the above-identified application and to transact all business in the United States Patent and Trademark Office in connection therewith:

Customer Number 27869

Please direct all telephone calls to:

Gerald P. Parsons
Telephone No.: (415) 217-6000
Fax No.: (415) 434-0646

ASSIGNEE CERTIFICATION UNDER 37 CFR 3.73(B)

The undersigned representative of the above-identified assignee certifies that the above-identified assignee is the assignee of the entire right, title and interest in the above-identified

patent application by virtue of a chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee as shown below:

1. From: SanDisk Corporation to Jian Chen and Khandker Quader, for which a copy thereof is attached.

The undersigned (whose title is supplied below) is empowered to sign this certificate on behalf of the above-identified assignee.

4/8/03
Date

Name: Charles Van Ouden
Title: VP; General Counsel

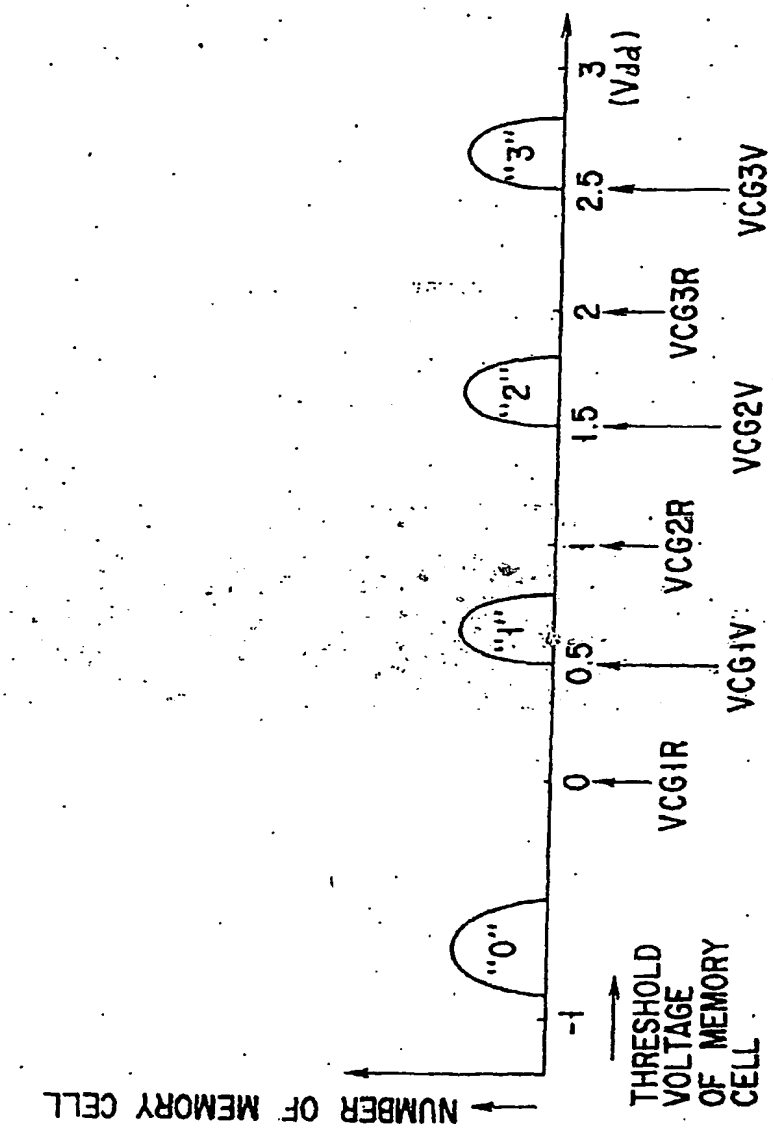


FIG. 1
(PRIOR ART)

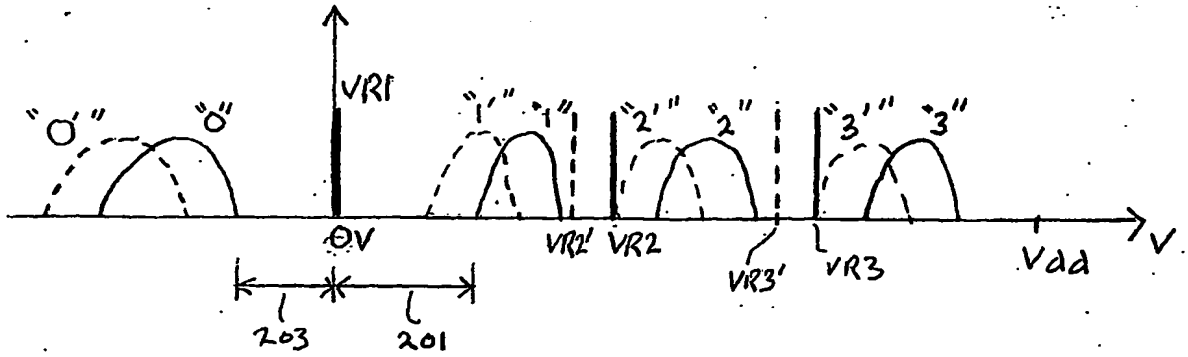
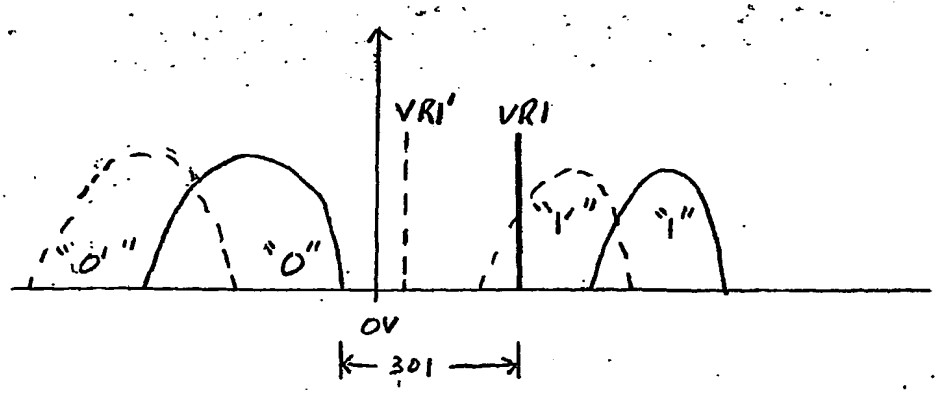


FIGURE 2 (PRIOR ART)



FIGUR3

10/1,4132 -041403

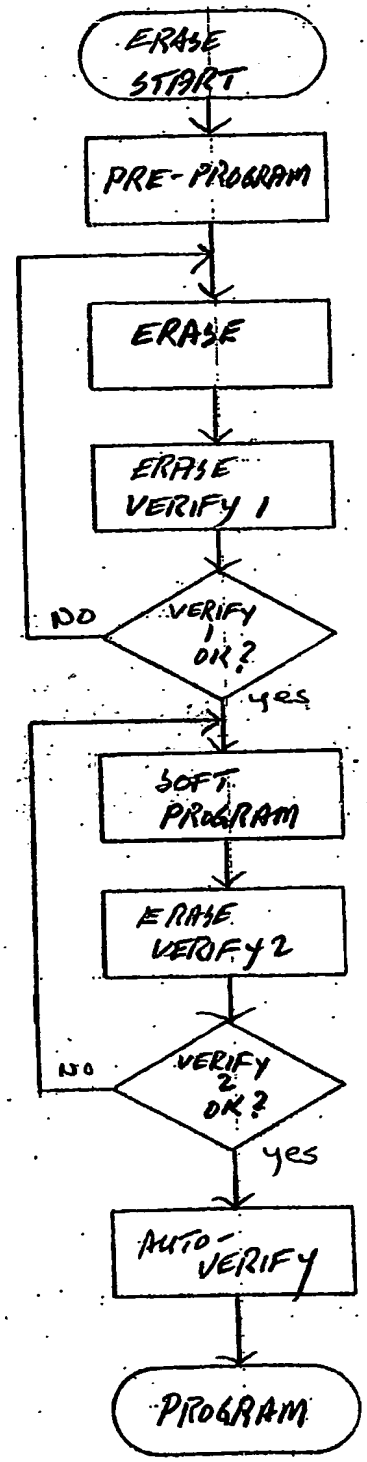


FIGURE 4

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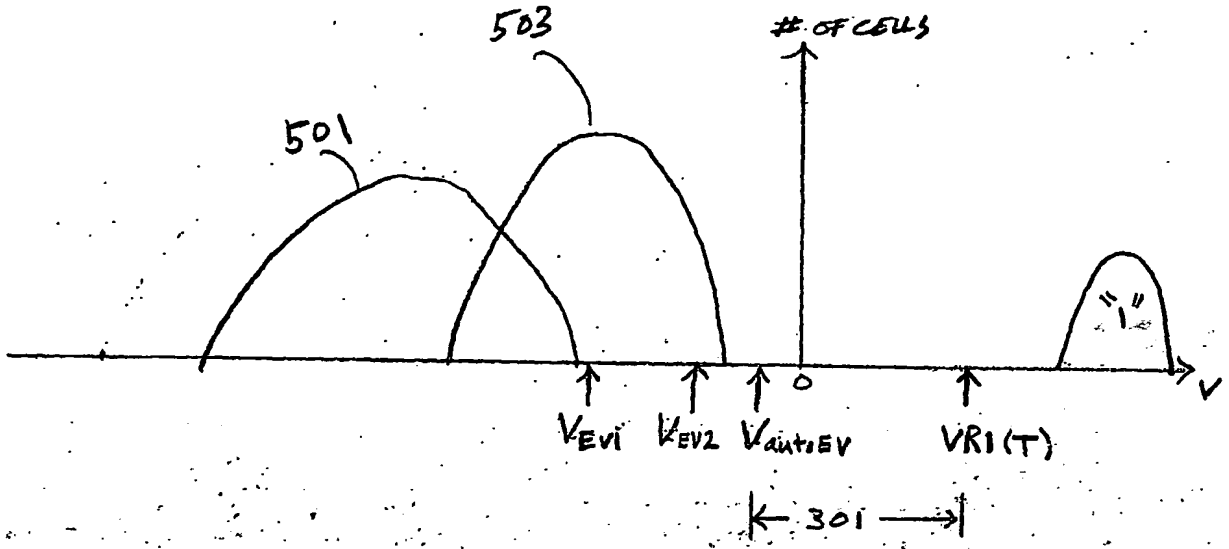

FIGURE 5

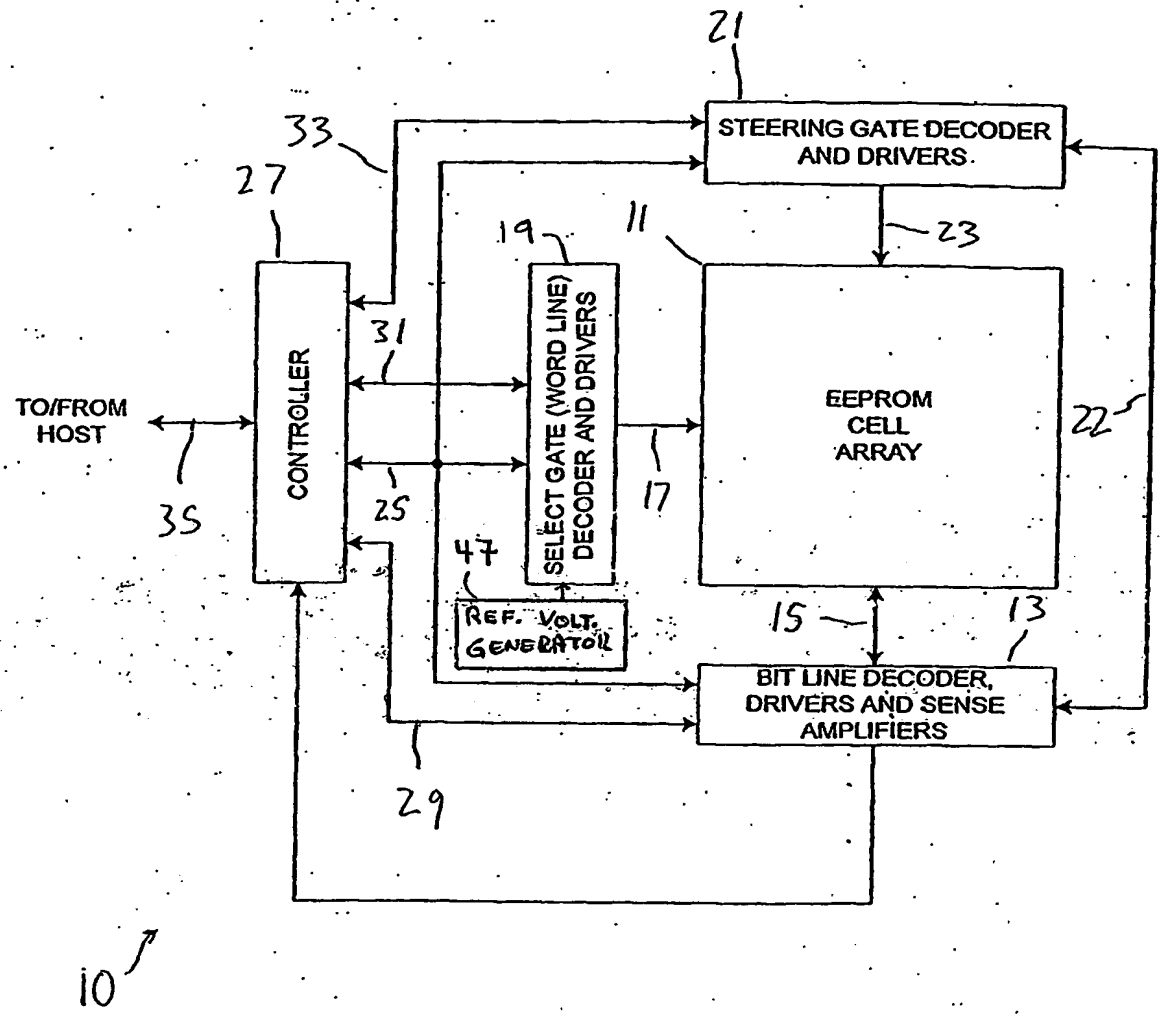

FIG. 6

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